PATENT APPLICATION
DOCKET NO.: 10012773-1

AMENDMENTS TO THE SPECIFICATION

Please replace the section having the heading "CROSS-REFERENCE TO RELATED APPLICATIONS(S)" on Page 1 of the original specification with the following amended section:

CROSS-REFERENCE TO RELATED APPLICATION(S)

This application discloses subject matter related to the subject matter disclosed in the following commonly owned co-pending patent application(s): (i) "System And Method For Synchronizing Data Transfer Across A Clock Domain Boundary," filed _____, ~~Ser. No.: _____~~ June 22, 2001; Application No.: 09/887,793 (Docket Number 10010788-1), in the name(s) of: Richard W. Adkisson, which is(are) hereby incorporated by reference for all purposes.

Please replace the paragraph starting from page 11, line 15 through page 12, line 2 with the following amended paragraph:

FIG. 4 depicts an exemplary clock state diagram including the states indicative of different amounts of phase difference between the exemplary primary and secondary clock signals having a 5:4 frequency ratio. Where there is no phase difference (i.e., normal condition), the clocks are in State 0 (reference numeral 400). Reference numerals 402, 404, 406, and 408 refer to the four positive clock states and reference numerals 403, 405, 407, and [[408]] 409 refer to the four negative clock states described hereinabove. It should be appreciated by those skilled in the art that since a full cycle period of skew is identical to the original clock state, the SYNC adjuster 305 of the clock synchronizer controller 120 can theoretically compensate for an infinite amount of skew between CLK1 and CLK2. Moreover, it should be apparent to those skilled in the art that [-1 State] is identical to [+4 State], [-2 State] is identical to [+3 State], [-3 State] is identical to [+2 State], and [-4 State] is identical to [+1 State].

Please replace the paragraph starting from page 17, line 16 through page 18, line 11 with the following amended paragraph:

Referring now to FIGS. 8A and 8B which together form FIG. 8, depicted therein is a further exemplary embodiment of a clock synchronizer controller 800 having a SYNC compensator circuit [[802]] 801 and jitter cycle delay compensation circuit 813 for providing SYNC pulse sampling and jitter compensation in accordance with the teachings of the present invention. Upon generating the SYNC pulse 108 and propagating it through appropriate flip-flop and distributor circuitry 302/304 as described above, it is provided to the SYNC compensator circuit [[802]] 801. As the clock frequency ratio is known (due to the Ratio Detect block 308), cycle 0 as defined by the compensated/corrected SYNC pulse in State 0 is expected in the middle of a time window demarcated by a plurality of timing registers, e.g., registers 802, 806 and 810. When SYNC correct is sampled, it is thus expected to exhibit a "010" binary sequence. If, for instance, the SYNC correct is sampled to be all zeros (indicating a lost SYNC pulse), a binary "1" is inserted in the middle by activating a MUX 808 so as to restart the SYNC pulse in the appropriate timing window. When a duplicate pulse condition is signified by obtaining "011" or "110" sequence, the extra "1" at

the ends is masked by activating logic such that only one properly timed SYNC pulse remains in the timing window. For example, when the "011" sequence is encountered, MUX 812 is activated so as to replace "1" at the right end with a "0". Similarly, when the "110" sequence is encountered, MUX 804 is activated so as to replace "1" at the left end with a "0".

Please replace the paragraph starting from page 19, line 29 through page 20, line 10 with the following amended paragraph:

As shown in FIG. 8B, the compensated SYNC pulse signal from the jitter cycle delay compensator 813 is provided to the Tapline and Selection block 316 which drives a control logic block 830 operable to generate the control signals described in greater detail hereinabove. In the particular exemplary embodiment depicted in this FIG., eleven delay registers, T0 through [[T11]] T10, are illustrated. Outputs from each of the delay registers are provided to the control logic circuit 830 for facilitating appropriate timing relationships among the control signals generated. Further, similar to the exemplary embodiment depicted in FIG. 3, the control logic provides appropriate timing information to the State and Correct block 310.